IN THE CLAIMS

1-19. (Cancelled)

20. (Previously presented) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a height equal to the second thickness of the inner leads, and wherein the peripheral part protrudes only in a direction toward the second semiconductor chip.

21. (Original) An ultra-thin semiconductor package device according to claim 20, wherein the die pad is disposed below the leads.

22. (Previously presented) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part, the peripheral part protruding towards only one of the first and second semiconductor chips;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a height equal to the second thickness of the inner leads, and wherein the bonding wires connected to the one of the first and second semiconductor chips are shorter than the bonding wires connected to the other semiconductor chip.

23. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein the bonding wires are connected by balls formed on the leads and stitches formed on the electrode pads.

24. (Original) An ultra-thin semiconductor package device according to claim 23, wherein metal bumps are formed on the electrode pads and wherein the stitches are formed on the metal bumps.

25. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein the die pad comprises divided first and second die pads.

26. (Original) An ultra-thin semiconductor package device according to claim 25, wherein the first and second die pads each include a corresponding chip attaching part and a corresponding peripheral part.

27. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

28. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein a thickness of the package body is about 580 μm, a thickness of the die pad peripheral part is about 100 μm, and a thickness of the chip attaching part is about 40 μm.

29. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

30-49. (Cancelled)

50. (Previously presented) An electronic apparatus including a semiconductor package device having a package body of less than 0.7 mm of thickness, said semiconductor package device comprising:

a lead frame including a die pad, a plurality of single-layer leads disposed around the die pad, and a tie bar disposed around and connected to the die pad, wherein said die pad includes a chip attaching part and a peripheral part surrounding the chip attaching part, the chip attaching part and the peripheral part having the same thickness;

a semiconductor chip having a plurality of electrode pads formed on an active surface of the chip, said chip connected to the chip attaching part, the peripheral part protruding away from the die pad chip attaching part only in a direction away from the semiconductor chip;

a package body for encapsulating the semiconductor chip;

bonding wires encapsulated by the package body, said bonding wires configured to electrically connect the electrode pads of the semiconductor chip to the leads, wherein each of the plurality of single-layer leads comprises an inner lead bonded to the bonding wire and encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body; and

wherein the chip attaching part has a first thickness and the inner lead has a second thickness that is greater than the first thickness.

51. (Original) An electronic apparatus according to claim 50, wherein the electronic apparatus is a memory card.

52-70. (Cancelled)

71. (Previously presented) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of single-layer leads disposed around the die pad, wherein each of the plurality of single-layer leads comprises an inner lead and an

outer lead, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein each of the plurality of electrode pads is electrically connected to at least one of the plurality of single-layer leads with a bonding wire, the peripheral part protruding away from the die pad chip attaching part only in a direction away from the semiconductor chip;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and a portion of the inner leads having a second thickness greater than the first thickness, wherein the bonding wires are directly connected to the portion of the inner leads, and wherein the chip attaching part and the peripheral part have the same thickness.

72. (Cancelled)

73. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the first thickness is between about 30% to 50% of the second thickness.

74. (Previously presented) The ultra-thin semiconductor package device according to claim 71, further comprising another semiconductor chip attached to a back side of the chip attaching part.

75. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the die pad is located below the leads.

76. (Previously presented) The ultra-thin semiconductor package according to claim 71, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

77. (Previously presented) The ultra-thin semiconductor package device according to claim 76, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

78. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

79. (Previously presented) The ultra-thin semiconductor package device according to claim 75, wherein the tie bar has the same thickness as the leads.

80. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the tie bar has the same thickness as the die pad peripheral part.

81. (Cancelled)

82. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the die pad comprises divided first and second die pads.

83. (Previously presented) The ultra-thin semiconductor package device according to claim 82, wherein the first and second die pads each include a chip attaching part and a peripheral part.

84. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

85. (Previously presented) The ultra-thin semiconductor package device according to claim 76, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

86. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

87. (Previously presented) A semiconductor package device comprising:

a lead frame that includes a die pad, leads disposed around the die pad, and tie bars connected to the die pad, the die pad including a chip attaching part having a first thickness and a peripheral part surrounding the chip attaching part;

an upper and a lower semiconductor chip that include electrode pads connected to the leads by bonding wires, the upper semiconductor chip bonded to an upper surface of the chip attaching part and the lower semiconductor chip bonded to a lower surface of the chip attaching part, the peripheral part protruding only in a direction towards the lower semiconductor chip; and

a package body that encapsulates the upper and the lower semiconductor chips, the die pad, the bonding wires, and a portion of the leads to define inner leads that are disposed inside the package body and outer leads that are disposed outside the package body, the inner leads having a second thickness that is greater than the first thickness.

88. (Cancelled)

89. (Previously presented) The semiconductor package device according to claim 87, wherein the plurality of leads are formed of a single layer.

90. (Previously presented) The semiconductor package device according to claim 87, wherein the first thickness is between about 30% to 50% of the second thickness.

91. (Previously presented) The semiconductor package according to claim 87, wherein the bonding wires are connected to the leads by balls formed on the surface of the leads and wherein the bonding wires are connected to the electrode pads by stitches formed on the electrode pads.

92. (Previously presented) The semiconductor package device according to claim 91, wherein a metal bump is formed on the electrode pads and the stitches are formed on the metal bumps.

93. (Previously presented) The semiconductor package device according to claim 87, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

94. (Previously presented) The semiconductor package device according to claim 87, wherein the tie bars have the same thickness as the leads.

95. (Previously presented) The semiconductor package device according to claim 87, wherein the tie bars have the same thickness as the peripheral part.

96. (Previously presented) The semiconductor package device according to claim 87, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the second thickness.

97. (Previously presented) The semiconductor package device according to claim 87, wherein the die pad comprises divided first and second die pads.

98. (Previously presented) The semiconductor package device according to claim 97, wherein the first and second die pads each include a chip attaching part and a peripheral part.

99. (Previously presented) The semiconductor package device according to claim 87, wherein an adhesive bonds the first and the second semiconductor chips to the chip attaching part.

100. (Previously presented) The semiconductor package device according to claim 99, wherein the first and the second semiconductor chips are memory devices and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

101. (Previously presented) The semiconductor package device according to claim 87, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

102-115. (Cancelled)

116. (Previously presented) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a first semiconductor chip mounted to a lower side of the chip attaching part and a second semiconductor chip mounted to an upper side of the chip attaching part, said first and second semiconductor chips having a plurality of electrode pads, the peripheral part perpendicular to the chip attaching part, the peripheral part having a lower surface that is parallel to but not coplanar with the lower side and an upper surface that is coplanar with the upper side, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads having a second thickness greater than the first thickness.

117. (Cancelled)

118. (Previously presented) The semiconductor package device of claim 50, wherein the first thickness is between about 30% to 50% of the second thickness.

119. (Cancelled)

120. (Previously presented) The semiconductor package device of claim 50 further comprising another semiconductor chip attached to a back side of the chip attaching part.

121. (Previously presented) The semiconductor package device of claim 50, wherein the die pad is located below the leads.

122. (Previously presented) The semiconductor package of claim 50, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and

wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

123. (Previously presented) The semiconductor package device of claim 122, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

124. (Previously presented) The semiconductor package device of claim 50, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

125. (Previously presented) The semiconductor package device of claim 121, wherein the tie bar has the same thickness as the leads.

126. (Previously presented) The semiconductor package device of claim 50, wherein the tie bar has the same thickness as the die pad peripheral part.

127. (Cancelled)

128. (Previously presented) The semiconductor package device of claim 50, wherein the die pad comprises divided first and second die pads.

129. (Previously presented) The semiconductor package of claim 128, wherein the first and second die pads each include a chip attaching part and a peripheral part.

130. (Previously presented) The semiconductor package device of claim 50, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

131. (Previously presented) The semiconductor package device of claim 122, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

132. (Previously presented) The semiconductor package device of claim 50, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

133. (Cancelled)

134. (Previously presented) The ultra-thin semiconductor package device of claim 74, wherein the semiconductor chip and the another semiconductor chip are of the same type.

135. (Previously presented) The ultra-thin semiconductor package device of claim 116, wherein the peripheral part protrudes from only one side of the chip attaching part.

136. (Previously presented) The ultra-thin semiconductor package device of claim 116, wherein the peripheral part protrudes upward from the chip attaching part.

137. (Previously presented) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

at least one semiconductor chip, the at least one semiconductor chip including a plurality of electrode pads, wherein the at least one semiconductor chip is bonded to a surface of the chip attaching part;

a package body encapsulating the at least one semiconductor chip; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads have a second thickness, wherein the first thickness is smaller than the second thickness, and wherein the peripheral part only protrudes downward.

138. (Previously presented) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a top surface of the chip attaching part.

139. (Previously presented) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a bottom surface of the chip attaching part.

140. (Previously presented) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a top surface of the chip attaching part, and wherein at least one other semiconductor chip is attached to a bottom surface of the chip attaching part.

141. (Previously presented) The ultra-thin semiconductor package device of claim 137, wherein the peripheral part has a thickness equal to the second thickness.

142. (Previously presented) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

a semiconductor chip, the semiconductor chip including a plurality of electrode pads, the semiconductor chip bonded to a surface of the chip attaching part, the peripheral part only protruding away from the semiconductor chip;

a package body encapsulating the semiconductor chip; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, the inner leads having a second thickness that is greater than the first thickness.